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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/067,410	02/04/2002	Christopher W. Hill	3380.1US (97-842.1)	8302

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EXAMINER

LEE, HSIEN MING

ART UNIT	PAPER NUMBER
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2823

DATE MAILED: 03/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/067,410

Applicant(s)

HILL ET AL.

Examiner

Hsien-Ming Lee

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-28 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-28 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-26 and 28-37 of U.S. Patent No. 6,372,643.

Although the conflicting claims are not identical, they are not patentably distinct from each other because both the Patent and the instant invention teach same subject matter except some minor obvious variations.

Particularly, the subject matter as recited in claims 1-28 of the instant invention are equivalent to that of claims 1-26 of the Patent, respectively. The obvious variations are that the Patent reciting "selectively depositing a self-aligned metal silicide contact directly onto an exposed, doped area of a semiconductor substrate" (independent claim 1, lines 3-5), whereas the instant invention reciting "depositing metal silicide directly onto at least one exposed, doped area of the semiconductor device structure" (independent claim 1, lines 3-4); and the Patent reciting "selectively depositing a layer of selective contact material directly onto a semiconductor substrate of an exposed, active device region of the semiconductor device" (independent claim 20, lines 3-5), whereas the instant invention reciting "depositing a contact material directly onto an exposed active device region of the semiconductor device structure" (independent claim 20, lines 3-4).

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The obvious variations do not render the instant invention to be patentably distinguishes it from the Patent. In addition, dependent claims 2-19 and 21-28 of the instant invention are substantially same as dependent claims 2-19 and 21-26 of the Patent.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 8-13, 15-17, 20 and 23-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hrzek (US 3,801,365) in view of Levine et al. (US 5,989,999).

In re claim 1, Hrzek in Fig. 3 and related text teaches the claimed method for fabricating an interconnect adjacent a contact of a semiconductor device structure, comprising:

- depositing metal silicide 78 directly onto at least one exposed, doped area 74 of the semiconductor device ^{structure}~~structure~~ without substantially depositing metal silicide 78 onto locations 73 of the semiconductor device structure that are laterally adjacent said at least one exposed, doped area 74; and
- depositing an interconnect material 80 or 80/86/82 onto said metal silicide 78.

In re claims 20, 27 and 28, Hrzek also teaches the claimed method for fabricating a selective contact and a local interconnect on a semiconductor device structure, comprising:

- depositing a contact material 78 (i.e. a selective contact material, metal silicide) directly onto an exposed active device region 74 of the semiconductor device structure without substantially depositing contact material 78 onto locations 73 of the semiconductor device structure that are laterally adjacent said exposed active device region 74; and

- depositing an interconnect material 80 or 80/86/82 onto said contact material 78.

In contrast, Hrzek is silent to as to depositing the interconnect material *in situ* with said depositing said contact material or said metal silicide.

However, Levine et al. in an analogous art teach utilizing *in situ* deposition technique for forming said metal silicide for the purposes of reducing contaminations and manufacturing units. (col.3, lines 39-48)

Therefore, one of the ordinary skill in the art at the time the invention was made would have been motivated to employ said *in situ* deposition technique as taught by Levine et al. for depositing the interconnect material *in situ* with depositing said contact material or said metal silicide since by this manner it would minimize undesirable contaminations and reduce manufacturing costs. (col.3, lines 39-48, Levine et al.).

In re claim 8, Hrzek in view of Levine et al. teaches the claimed method, as stated above, including said metal silicide comprising titanium silicide, wherein Hrzek further teaches utilizing titanium tetrachloride or titanium tetrabromide as metallic precursor for depositing said titanium silicide. (col.10, lines 19-20, 52-58, Hrzek)

In re claims 9 and 25, Hrzek in view of Levine et al. teaches the claimed method, as stated above, including that depositing said interconnect material 80 or 80/86/82 comprises blanket depositing said interconnect material 80 or 80/86/82, i.e. depositing said interconnect material 80 or 80/86/82 on said exposed, doped area 74 and said adjacent region 73. (Fig.3, Hrzek)

In re claims 10 and 26, Hrzek in view of Levine et al. teaches the claimed method, as stated above, further comprising patterning said interconnect material 80 over said contact material 78 as shown in Fig.3 in Hrzek.

In re claims 11 and 24, Hrzek teaches selectively depositing metal silicide 78 onto the exposed area 74 and depositing the interconnect material 80 onto the metal silicide 78 as shown in Fig.3.

Hrzek further indicates that when the exposed area is as deep as the depth of 64 (Fig.2), more silicide layers can be selectively depositing onto the exposed area 64, as the silicide layer 68 has not reached the edge of the exposed area 64.

Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to further selectively depositing said interconnect material 80 after selectively depositing said metal silicide 78, in light of the teaching shown in Fig.2, since by doing so it would eliminate a step of patterning said interconnect material, which, in turn, would simplify manufacturing processing.

In re claims 12, 13 and 23, Hrzek in view of Levine et al. also teaches depositing a layer 82/86 of electrically conductive material (i.e. Al and Mo) over said interconnect material 80 (Fig.3, Hrzek); and further patterning said layer 82/86 as the same manner as patterning a layer 102 using a photoresist layer (Fig.4 and col. 14, lines 19-23).

In re claims 15 and 17, Hrzek in view of Levine et al. further teaches depositing said metal silicide (i.e. molybdenum silicide) comprising reacting a metallic precursor (i.e. such as molybdenum pentachloride; col.8, lines 64-67, Hrzek) with a silicon-containing compound (i.e. SiCl_4 , col.9, line 21, Hrzek).

In re claim 16, Hrzek in view of Levine et al. also teaches the claimed method, as stated above, further comprising reacting a metallic precursor comprising the titanium tetrahalide (i.e. titanium tetrachloride; col.10, lines 19-20, 52-58, Hrzek) if the metal silicide is the titanium silicide.

4. Claims 2-5, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hrzek (US '365) in view of Levine et al. (US '999) as applied to claims 1, 8-13, 15-17, 20 and 23-28 above, and further in view of Chang et al. (US 5,043,299).

In re claims 2-4 and 21, Hrzek in view of Levine et al. teaches the claimed method, as stated above, but fails to teach exposing said at least one exposed, doped area of the semiconductor device

structure to a plasma comprising an activated species of at least one of nitrogen, hydrogen, and ammonia; and cleaning the semiconductor device structure.

Chang et al. in an analogous art of selective deposition teach a pre-deposition preparation by exposing the exposed, doped area of the semiconductor device structure to plasma comprising an activated species of at least one of nitrogen and hydrogen (Fig.1 and text in col. 3, lines 14-26; col. 4, lines 10-15); and cleaning the semiconductor device structure (col.7, lines 1-11) for the purpose of removing contaminants including undesirable oxide and moisture (col.2, lines 15-28; col.6, lines 48-61).

Therefore, one of the ordinary skill in the art at the time the invention was made would have been motivated to expose the exposed, doped area of semiconductor device structure of Hrzek in view of Levine et al. by the plasma comprising either nitrogen or hydrogen and cleaning the semiconductor device structure, as taught by Chang et al., since by doing so it would be beneficial to the subsequent selective deposition. (col.2, lines 15-28; col.6, lines 48-61, Chang et al)

In re claim 5, Hrzek in view of Levine et al. and further in view of Chang et al. further teach that said cleaning includes employing a cleaning agent comprising chlorine. Particularly, Chang et al. indicate using a halogen-containing gas, which at least would include chlorine and fluorine, for the cleaning purpose. (col.7, lines 5-6).

In re claim 22, Hrzek in view of Levine et al. and further in view of Chang et al. do not teach exposing the semiconductor device structure to a nitrogen-ammonia plasma. However, the selection of the cleaning plasma for said exposing step is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). For example, the

cleaning plasma can be selected for the particular surface to be cleaned, dependent upon the material of the particular surface. (col.3, lines 14-26, Chang et al.) In this case, the applicant is required to demonstrate the criticality, generally by showing that the claimed plasma would achieve unexpected results relative to the prior art. See M.P.E.P. 2144.05 III.

5. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hrzek (US '365) in view of Levine et al. (US '999) as applied to claims 1, 8-13, 15-17, 20 and 23-28 above, and further in view of Kolar et al. (US 5,162,259).

Hrzek in view of Levine et al. teaches the claimed method, as stated above, but fails to teach cleaning the semiconductor device structure after said depositing said metal silicide, wherein said cleaning includes employing a cleaning agent comprising at least one of chlorine, hydrochloric acid, and hydrofluoric acid.

Kolar et al. in an analogous art teach forming a silicide layer 40 followed by cleaning the semiconductor device structure employing a cleaning agent comprising hydrochloric acid, prior to depositing an interconnect material 38. (Fig.4 and text in col. 21-23)

Therefore, one of the ordinary skill in the art at the time the invention was made would have been motivated to utilize said hydrochloric acid as cleaning agent as taught by Kolar et al., in the method of Hrzek in view of Levine et al. to clean the surface of said deposited metal silicide and then to deposit said interconnect material, since by doing so it would improve the adhesion between adjacent layers.

6. Claims 14, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hrzek (US '365) in view of Levine et al. (US '999) as applied to claim 1 above, and further in view of Park et al. (US 6,087,257).

In re claim 14, Hrzek in view of Levine et al. teaches the claimed method but fails to teach that depositing said interconnect material comprises depositing at least one of titanium and titanium nitride.

However, Park et al. in an analogous art teach forming a titanium silicide 14 onto an exposed, doped area 12 of a semiconductor substrate 10; depositing said titanium nitride 15; and depositing an electrically conductive layer 16 onto said titanium nitride 15, wherein said titanium nitride 15 acts as a diffusion barrier layer (Fig. 1E and text in col.1, lines 50-58, Park).

Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to deposit said titanium nitride as said interconnect material, when the underlying metal silicide is said titanium silicide as taught by Park et al., after selectively depositing said metal silicide of Hrzek; and further to proceed the deposition of said electrically conductive layer since the selection of said interconnect material depends on the function of the device and the adjacent materials, as evidenced by Park et al. By depositing said titanium nitride as said interconnect material on said titanium silicide, prior to depositing said electrically conductive layer thereon, it would avoid diffusion problem between said titanium silicide and said electrically conductive layer. (col.1, lines 50-58, Park)

In re claims 18 and 19, Hrzek teaches the claimed method, as stated above, but fails to teach that depositing said interconnect material comprises reacting a metallic precursor with a reactant comprising at least one of ammonia, nitrogen trifluoride, an organic silane reactive gas, and an activated species; and said reacting a metallic precursor comprises at least one of a titanium tetrahalide and a $Ti(NR_z)_4$, where R is selected from the group consisting of hydrogen and alkyl groups, with said reactant.

However, Levine et al. in an analogous art of forming said titanium nitride (i.e. same material as said interconnect material in Hrzek and Park et al.) teach reacting a metallic precursor (i.e.

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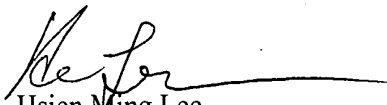
TDMAT) with a reactant (i.e. a reactive gas), wherein said metallic precursor comprises a $Ti(NR_z)_4$, where R is selected from the group consisting of hydrogen and alkyl groups, with said reactant. (col.1, line 58 through col.2, line 13).

Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to deposit said interconnect material (i.e. titanium nitride) of Hrzek and Park et al. by reacting said metallic precursor with said reactant, as taught by Levine et al., since by this manner it would produce said interconnect material having satisfactory barrier function with improved resistivity. (col.3, lines 58-65, Levine et al.)

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-0142 for regular communications and 703-305-0142 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



Hsien Ming Lee
March 8, 2003